CLAIMS

1. A programmable memory cell useful in a memory array having column bitlines and row wordlines, the memory cell comprising:

a transistor having a gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate; and

wherein the second doped semiconductor region of the transistor is connected to one of said row wordlines, and wherein said gate dielectric is formed such that the gate dielectric is more susceptible to breakdown near the first doped semiconductor region than said second doped semiconductor region.

2. The memory cell of Claim 1 wherein said row wordlines are formed from a buried N+ layer.

3. The memory cell of Claim 1 wherein the gate dielectric of the transistor is thicker proximal to the second doped semiconductor region than to the first doped semiconductor region.

4. The memory cell of Claim 1 wherein the gate dielectric of the transistor is damaged by ion implantation near said first doped semiconductor region.

5. The memory cell of Claim 1 wherein said gate is formed from one of said column bitlines.

6. The memory cell of Claim 1 wherein said memory cells further including a programmed doped region formed in said substrate in said channel region when said memory cell has been programmed.

7. A method of operating a programmable memory array comprising a plurality of row wordlines, a plurality of column bitlines, and a plurality of memory cells at respective crosspoints of the row lines and column lines, said memory cells comprising a transistor having a gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate, the gate being formed from one of said column bitlines, and the second doped semiconductor region of the transistor connected to one of said row wordlines, said gate dielectric formed such that the gate dielectric is more susceptible to breakdown near the first doped semiconductor region than said second doped semiconductor region, the method comprising:

applying a first voltage to a selected one of the column bitlines and gate of a selected transistor; and

applying a second voltage to a selected one of the row wordlines;

wherein the first voltage and the second voltage form a potential difference across the gate dielectric of said selected transistor to cause the formation of a programmed doped region in said substrate in said channel region of said selected transistor.

8. The method of Claim 7 wherein said selected transistor is read by applying a fourth voltage on the gate of said selected transistor and monitoring for a current flowing from said gate to said selected column bitline.

9. A programmable memory array comprising a plurality of row wordlines, a plurality of column bitlines, and a plurality of memory cells at respective crosspoints of the row wordlines and column bitlines, each of the memory cells comprising:

a transistor having a gate, a gate dielectric between the gate and over a substrate, and first and second doped semiconductor regions formed in said substrate adjacent said gate and in a spaced apart relationship to define a channel region therebetween and under said gate, the gate being formed from one of said column bitlines; and

wherein the second doped semiconductor region of the transistor is connected to one of said row wordlines, said gate dielectric is formed such that the gate dielectric is more susceptible to breakdown near the first doped semiconductor region than said second doped semiconductor region.

10. The memory array of Claim 9 wherein said row wordlines are formed from a buried N+ layer.

11. The memory array of Claim 9 wherein said column bitlines are connected to said gate by a column bitline segment.

12. The memory array of Claim 9 wherein the gate dielectric of the transistor is thicker proximal to the second doped semiconductor region than to the first doped semiconductor region.

13. The memory array of Claim 9 wherein the gate dielectric of the transistor is damaged by ion implantation near said first doped semiconductor region.

14. The memory array of Claim 9 wherein said memory cells further including a programmed doped region formed in said substrate in said channel region when said memory cell has been programmed.